Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

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1. (Currently Amended) A method of recovering ~~a clock signal and~~ data from a data signal comprising:

receiving the data signal having a first data rate;

receiving [[the]] a clock signal having a first clock frequency, and alternating between a first level and a second level;

generating a first signal by passing the data signal when the clock signal is at the first level, and storing the data signal when the clock signal is at the second level;

generating a second signal by passing the data signal when the clock signal is at the second level, and storing the data signal when the clock signal is at the first level;

generating a third signal by passing the first signal when the clock signal is at the second level, and storing the first signal when the clock signal is at the first level;

generating a fourth signal by passing the second signal when the clock signal is at the first level, and storing the second signal when the clock signal is at the second level;

generating an error signal by taking an exclusive-OR of the first signal and the second signal; and

generating a reference signal by taking an exclusive-OR of the third signal and the fourth signal,

wherein the first data rate is twice the first clock frequency.

2. (Original) The method of claim 1 further comprising:

applying the error signal and the reference signal to a charge pump to generate a charge pump output.

3. (Original) The method of claim 2 wherein the generating the first signal is done by a first latch, the generating the second signal is done by a second latch, the generating the third signal is done by a third latch, and the generating the fourth signal is done by a fourth latch.

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4. (Original) The method of claim 3 wherein the generating the error signal and the generating the reference signal is done by an exclusive-OR gate.

5. (Original) The method of claim 1 wherein the third signal and the fourth signal are demultiplexed data outputs.

6. (Original) The method of claim 5 wherein the clock signal has approximately a fifty percent duty cycle.

7. (Original) The method of claim 5 wherein the clock signal is generated by a ring oscillator.

8. (Original) An apparatus for recovering data from a received data signal comprising:

a first storage device configured to generate a first signal by receiving the received data signal, and either passing the received data signal or storing the received data signal;

a second storage device configured to generate a second signal by receiving the received data signal, and either passing the received data signal or storing the received data signal;

a third storage device configured to generate a third signal by receiving the first signal, and either passing the first signal or storing the received first signal;

a fourth storage device configured to generate a fourth signal by receiving the second signal, and either passing the second signal or storing the second signal;

a first logic gate configured to perform an exclusive-OR of the first signal and the second signal;

and a second logic gate configured to perform an exclusive-OR of the third signal and the fourth signal,

wherein when the first storage device passes the received data, the second storage device stores the received data, the third storage device stores the first signal, and the fourth storage device passes the second signal, and when the first storage device stores the received data, the second storage device passes the received data, the third storage device passes the first signal, and the fourth storage device stores the second signal.

9. (Original) The apparatus of claim 8 wherein the first storage device either passes or stores the received data signal under control of a clock signal, the second storage device either passes or stores the received data under control of the clock signal, the third storage device either passes or stores the first signal under control of the clock signal, and the fourth storage device either passes or stores the second signal under control of the clock signal.

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10. (Original) The apparatus of claim 9 wherein the first storage device passes the received data signal when the clock is high, stores the received data signal when the clock is low.

11. (Original) The apparatus of claim 9 wherein the clock signal is a differential clock signal.

12. (Original) The apparatus of claim 11 wherein the clock signal has approximately a fifty percent duty cycle.

13. (Original) The apparatus of claim 11 wherein the clock signal is generated by a ring oscillator.

14. (Original) An apparatus for recovering data from a received data signal comprising:

a first storage device having a data input coupled to a data input port, a clock input coupled to a first clock port, and an output;

a second storage device having a data input coupled to the data input port, a clock input coupled to a second clock port, and an output;

a third storage device having a data input coupled to the output of the first storage device, a clock input coupled to the second clock port, and an output;

a fourth storage device having a data input coupled to the output of the second storage device, a clock input coupled to the first clock port, and an output;

a first exclusive-OR gate having a first input coupled to the output of the first storage device and a second input coupled to the output of the second storage device;

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and a second exclusive-OR gate having a first input coupled to the output of the third storage device and a second input coupled to the output of the fourth storage device,

wherein the first, second, third, and fourth storage devices couple a signal at the data input to the output when a voltage on the clock input is a high, and the first, second, third, and fourth storage devices store a signal at the data input when the voltage on the clock input is a low.

15. (Original) The apparatus of claim 14 wherein the data input port is configured to receive a differential signal.

16. (Original) The apparatus of claim 15 wherein the first clock port receives a clock signal.

17. (Original) The apparatus of claim 16 wherein the second clock port receives a complement of the clock signal.

18. (Original) An optical receiver comprising the apparatus of claim 14.

19. (Original) An optical transceiver comprising:

an optical transmitter; and

the optical receiver of claim 18 coupled to the optical transmitter.

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20. (Original) A system for receiving and transmitting optical signals comprising:

a light emitting diode, configured to transmit optical signals;

a transmitter coupled to the light emitting diode;

a photo-diode, configured to receive optical signals;

a receive amplifier coupled to the photo-diode;

the apparatus of claim 14 coupled to the receive amplifier; and

a media access controller coupled to the apparatus of claim 14.

21. (Currently Amended) A clock and data recovery apparatus comprising:

a voltage controlled oscillator, configured to provide a clock signal at a clock output;

a half-rate phase detector comprising a data input, configured to receive a data input signal having a data rate and a data pattern, and a clock input coupled to the clock output of the voltage controlled oscillator, configured to receive the clock signal; and

a low-pass filter coupled between the half-rate phase detector and the voltage controlled oscillator,

a charge pump coupled between the half-rate phase detector and the low-pass filter,

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wherein the clock signal has a frequency which is half the data rate, and the half-rate phase detector provides a first signal and a second signal, the first signal dependent on the phase difference between the data input signal and the clock signal, and also dependent on the data pattern, the second signal dependent on the data pattern,

wherein the charge pump combines the first signal and the second signal to generate an output signal that is dependent on the phase difference but is not dependent on the data pattern.

22. (Currently Amended) The apparatus of claim 21 ~~further comprising a charge pump coupled between the half-rate phase detector and the low-pass filter,~~

wherein the charge pump generates [[an]] the output signal by subtracting the second signal from the first signal.

23. (Original) The apparatus of claim 22 wherein the clock signal has approximately a fifty percent duty cycle.

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24. (Original) The apparatus of claim 22 wherein the voltage controlled oscillator comprises a ring oscillator.